Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Canceled)

3. (New) A normally on NMOS field effect transistor comprising:

a source formed by a source material,

a drain formed by a drain material, and

a channel formed by a channel material,

the source, the drain and the channel materials being selected such that:

an electronic affinity of the drain material is lower than an electronic affinity of the channel material, and

an electronic affinity of the source material is higher than the electronic affinity of the channel material.

4. (New) A normally on PMOS field effect transistor comprising:

a source formed by a source material,

a drain formed by a drain material, and

a channel formed by a channel material,

the source, the drain and the channel materials being selected such that:

an upper level of a valence band of the drain material is higher than an upper level of a valence band of the channel material and, and

an upper level of a valence band of the source material is lower than the upper level of the valence band of the channel material.

5. (New) An integrated circuit, comprising:

normally on PMOS type; and

normally on NMOS type field effect transistors, wherein:

the normally on NMOS field effect transistor comprises:

an NMOS source formed by an NMOS source material,

an NMOS drain formed by an NMOS drain material, and

an NMOS channel formed by an NMOS channel material,

the NMOS source, NMOS drain and NMOS channel materials being selected such that:

an electronic affinity of the NMOS drain material is lower than an electronic affinity of the NMOS channel material, and

an electronic affinity of the NMOS source material is higher than the electronic affinity of the NMOS channel material; and

the normally on PMOS field effect transistor comprising:

a PMOS source formed by a PMOS source material,

a PMOS drain formed by a PMOS drain material, and

a PMOS channel formed by a PMOS channel material,

the PMOS source, the PMOS drain and the PMOS channel materials being selected such that:

an upper level of a valence band of the PMOS drain material is higher than an upper level of a valence band of the PMOS channel material, and

an upper level of a valence band of the PMOS source material is lower than the upper level of the valence band of the PMOS channel material.